layers and insulated by a layer of gate insulating material from said first, second and third layers;

a word line comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer;

a bit line comprising a layer of conductive material formed [on the] such that all portions thereof are formed above said top surface of said substrate but formed so as to be in electrical contact with the surface of said first layer coincident with [the] said top surface of said substrate at each [cell] vertical MOS transistor in said array, and

a spacer layer of insulating material insulating said word line [contact] from said bit line[contact].

4. The apparatus of claim 3 wherein said bit line contact contacts said first layer at all points between said spacer layers of the word line contacts of adjacent memory cells.

5. The apparatus of claim 3 wherein said bit line contact contacts said first layer at at least some points between said spacer layers of the word line contacts of adjacent memory cells and runs over the top of said word line and is insulated therefrom by said spacer layer.

Remarks

Amendments To Respond To Definiteness Rejections

In response to the rejections under 35 U.S.C. §112, claim 2 has been amended to clarify what structures are intended to be coincident with each other. An amendment has been made to claim 2 to specify that the second layer of insulation completely covers said

word line. The amendments to claim 2 are believed to clarify that the three dimensional drain region is formed within the substrate so as to have a two dimensional surface coincident with the two dimensional surface of the substrate. A similar amendment has been made to claim 3. Claim 3 has been amended in original lines 22-23 to replace "word line contact" with "word line" and replace "bit line contact" with "bit line" to provide antecedent basis.

Amendments To Clarify Misinterpreted Claim Limitations

The remaining amendments made in this response were made necessary by the Examiner's final rejection in which the Examiner misinterpreted certain key limitations in all the rejected claims and misinterpreted the teachings of the prior art. Because these errors did not become apparent until the applicant amended the claims to specify that the floating gate was self aligned and the Examiner responded with a final rejection mistakenly holding that the Mori reference teaches a self aligned floating gate when it, in fact, does not, this response to the final rejection could not have been presented earlier because it was not apparent that mistakes had been made until the final rejection was imposed.

Some minor amendments to the language of the independent claims to clarify the intended meaning of the limitations which have been misinterpreted are presented herewith, and applicant's believe that under the provisions of 37 CFR 1.116(b) they are entitled to have the amendments considered. Applicant's believe that good and sufficient reason exists to have these amendments entered. The applicant's believe that the amendments made herein are necessary because the claim limitations, as they existed before this amendment, obviously did not correctly convey to the Examiner their true intended meaning as evidenced by the Examiner's misinterpretation of them and

misapplication of the prior art to them.

The amendments could not have been made earlier. The applicant's could not have known that the Examiner was going to misinterpret the self aligned limitation and misapply the prior art to it until the amendment to specify the floating gate as misaligned was actually made. That did not happen until the response to the first Office Action. Accordingly, the amendments are necessary and could not have been presented earlier. The proposed amendments give the claim language direct support for the meaning that would be accorded the preamendment limitations by the Federal Circuit in interpreting the claims in light of the claim language itself, the specification and the prosecution history to date. The applicant's respectfully request that the amendments be entered.

THE PRIMA FACIE CASE OF OBVIOUSNESS HAS NOT BEEN PROPERLY ESTABLISHED BECAUSE THE CLAIM LANGUAGE HAS NOT BEEN PROPERLY CONSTRUED AND GIVEN PROPER WEIGHT

The "Self Aligned" Limitations in Claims 1, 2 and 3 and the dependent claims 4 and 5 Defining The Structure of the Floating Gate Has Not Been Construed Properly And Has Been Improperly Generalized

Claim 1 contained the following limitations defining the structure of the floating gate prior to this amendment (all three independent claims 1-3 still contain a self aligned limitation, albeit stated more clearly so as to avoid misinterpretation):

> said well having a floating gate of conductive material formed therein
> *which is self aligned* to not extend laterally beyond edges of said well

Claim 2 contained the following self alignment limitation prior to this amendment (and still contains a self aligned limitation):

> a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well

Claim 3 contained the following self alignment limitation prior to this amendment (and still contains a self aligned limitation):

> said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well

The Examiner seems to have construed this "self aligned" limitation in each independent claim in the final rejection as meaning solely that the floating gate material does not extend beyond the edges of the well. While that is an understandable mistake given the language of the limitation, that is not actually what the limitation means in light of the specification and drawings and the intent of the applicants.

The specification teaches that the self alignment of the floating gate is achieved in steps 33 and 34 of the process detailed in the table beginning at page 13. In step 33, the poly layer 102 is deposited, and, in step 34, the poly layer 102 is etched back *to remove all poly from horizontal surfaces*. This leaves the floating gate material deposited only on the vertical surfaces of the well or trench. The specification teaches:

> Next, a layer of P type doped polysilicon 102 is deposited over the complete structure from which the floating gate 22 in Figure 5 will be formed to leave the structure as shown in Figures 20A, B and C. Typically, about 1000 angstroms of polysilicon is deposited and is doped P type with chemical dope of phosphorous either during or after deposition to a resistivity of 50 ohms per square.
>
> To form the floating gate, the doped polysilicon is etched back off

all horizontal surfaces and part way down into the recessed gate windows 88 and 90 to leave the segments of polysilicon shown at 102 in Figure 21B. These segments of doped polysilicon 102 correspond to the floating gate 22 in the finished structure shown in Figure 5.

The drawings clearly show a self aligned floating gate which has no horizontal components either on the bottom of the well or overlying the gate oxide and top surface of the substrate at the top of the well.

These passages from the specification plus the drawings clearly teach that a self aligned floating gate, as that phrase is used in the claims is intended to convey a meaning of a floating gate inside the well but having conductive material only on the vertical sidewalls of the well with no conductive material on the bottom of the well or overlying any portion of the top surface of the substrate. Thus, in claims 1-5, the phrase self aligned floating gate structure should be interpreted by skilled artisans and the Federal Circuit as a floating gate with conductive material deposited only on the vertical surfaces of the well with no horizontal component on top of any oxide at the top edge of the well and no horizontal component at the bottom of the well.

Claim limitations are to be interpreted in accordance with the language of the claims themselves, the specification and drawings and the prosecution history. Markman v. Westview Instruments, Inc., 34 USPQ2d 1321 (Fed. Cir. 1995). Claims terms are to be given their ordinary meanings unless the specification has given them special meaning. Intellicall Inc. v. Phonometrics Inc., 21 USPQ2d 1383 (Fed. Cir. 1992). Here, there is no ordinary meaning for the term self aligned in vertically integrated structures because the process of self alignment of floating gates in vertical transistors is relatively new and the term is not believed to yet have an established

meaning to artisans. The term “self aligned” does have an established meaning in **planar** or horizontally constructed MOS structures. In planar MOS devices, a self aligned gate means that the edges of source and drain implants are aligned with the edges of spacer insulation layers formed at the edges of MOS gates by using the gate and spacers as an implant mask. But in vertical structures, this meaning does not apply and there is no evidence that the undersigned is aware of or the inventor is aware of that indicates that self alignment of a floating gate in a vertically integrated MOS device has any established meaning other than the meaning defined for the term in the applicant's specification. Accordingly, the meaning given the term “self aligned floating gate” in a vertical MOS device given in applicant's specificaiton should have been given this limitation by the Examiner in making out the prima facie case of obviousness and in considering the issue of interpretation. For the reasons given below, it is clear that this did not happen.

The Federal Circuit has clearly stated that even if a term has a meaning to an artisan which is different than the meaning assigned the term in the applicant's specification and prosecution history, the meaning given in the patent documents controls over any contrary or different meanings for the term commonly understood in the art. Southwall Technologies Inc. v. Cardinal IG Company, 34 USPQ2d 1673 (Fed. Cir. 1995).

The Examiner did not assign the self aligned limitation to proper meaning. The Examiner took the position in the final rejection at issue here that the Mori reference anticipates the claims. The Examiner took this position because Mori shows a floating gate in his drawings that apparently does not extend beyond the edges of the well. The Examiner assumed this is what the self aligned limitation meant when, it fact, it means

more than this, as described above. The Examiner apparently looked only at the drawings and must have missed the portion of Mori's specification (detailed below) where Mori clearly states that the floating gate is formed using a mask to pattern and etch the poly 1 layer. The self alignment process taught in the applicant's specification does not used a mask - it uses an etch that only attacks horizontal components and leaves vertical components unharmed. The omission of a mask has significant implications for density of the array as is detailed in the enclosed declaration of Madhu Vora who is the inventor and who has done a comparative study of the Mori cell structure and the cell structure taught in his patent specification.

The Examiner also rejected all the claims for obviousness over Mori standing alone. The Examiner's 102 rejection of claim 2 (which also contains the self aligned limitation) is clear evidence that the Examiner has misinterpreted the self aligned limitation. Such a misinterpretation of a claim is fatal to the prima facie case of obviousness. ACS Hosp. Sys. Inc. v. Montefiore Hosp., 221 USPQ2 929, 933 (Fed. Cir. 1985). Since the properly interpreted claim limitation is not met exactly, the anticipation rejection must fall also, and since the claim was misinterpreted, the prima facie case of obviousness has not yet been established properly.

The Examiner Has Misunderstood The Intended Meaning For the Self Aligned Limitation and the Applicability of Mori's Teachings To This Limitation

The Examiner Has Misunderstood the Technical Content of the Teachings of the Mori Reference

The Mori reference does not teach a self aligned floating gate because the Mori floating gate has a horizontal component at the bottom of the trench and horizontal

components at the top of the well overlapping the gate oxide layer. These components result because Mori does not teach use of an etch back to remove all horizontal components of the floating gate material as is taught in the applicant's specification.

If Mori taught the same invention as the applicant, there would be no horizontal component of the Mori floating gate either at the bottom of the well or above the gate oxide.

Further, Mori specifically teaches that the floating gate is formed by depositing first poly and then masking and etching to define the floating gates in each trench. At Col. 9 in the section entitled "2.3. Gate Conductor Formation", at lines 23 through 29, Mori teaches:

> "The poly 1 deposition forms a conductive layer within each trench, including a vertically extending section 82. The vertically extending section 82 covers the gate oxide 74 on the sidewalls of the trench, leaving a central cavity 84 in the trench.
>
> The poly 1 layer is then patterned and etched to define the floating gates."

Those skilled in the art know that the process being referred to in the quoted passage is a process which uses a mask to define the limits of the floating gate and is not a self aligned process. Self aligned processes do not use masks, and that is why they are preferred over process steps using masks because in self aligned processed, there are no registration errors. Further, there does not need to be any extra space left between structures to accomodate registration errors in a self aligned process. See the discussion in the next section for the significance of the difference in structure which results from applicant's self aligned process in terms of advantages it creates.

The "Self Aligned" Limitation In the Claimed Structure Gives Rise To

Several Advantages Over the Mori Prior Art

Dens r Array With Mor Tightly Pack d Cells

Whenever a mask is used, more chip area must be consumed because the mask can have alignment errors on registration and extra space must be left between the proposed boundaries of the structure to be formed with the mask and adjacent structures so that registration errors do not cause adjacent structures to be affected by the process step or steps involving the mask in ways not intended. These cushions that Mori would have had to leave in constructing his floating gates use up die area and reduce the density of the array as compared to the self aligned floating gate formation process of the Vora patent application at bar. The difference in array density caused by this structural difference as well as the structural differences to be described below regarding the lack of a buried bit line in the claimed invention at bar lead to dramatic differences in array density, as pointed out in the declaration of Madhu Vora attached hereto.

Lower Programming Voltage Because Less Parasitic Capacitance Between the Floating Gate and the Drain and the Floating Gate and the Source

The lack of a self aligned floating gate in Mori causes Mori's programming voltage to be higher. This is a bad think in very dense EEPROM arrays because higher programming voltages require separate power supplies or more complicated step up circuitry to raise the voltage of the Vcc supply. Higher programming voltages also require thicker insulation layers everywhere the programming voltage goes on the chip so as to prevent punch through and destruction of the chip.

Mori's program voltage is higher than the programming voltage of the applicant's cell for the following reason. The lack of a self aligned floating gate in the

Mori device causes horizontal components of floating gate material to exist at the bottom of the well an at the top of the well. The horizontal component at the bottom of the well gives rise to a parasitic capacitance from the floating gate to the source. The horizontal component at the top of the well gives rise to a parasitic capacitance between the floating gate and the drain. The two parasitic capacitances create an equivalent circuit which is like that shown in Figure 3 of applicant's drawings with the two parasitic capacitances connected in parallel to C1. The two additional parasitic capacitances in the Mori device add to the capacitance C1 and make it larger relative to the capacitance of C2. The programming tunnelling to the floating gate occurs when a program voltage of some voltage such as 15 volts is applied to line 47 and a lower voltage, say 8 volts, is applied to the source line 49 in Figure 3. C2 and C1 form a voltage divider between the voltage on line 47 and the voltage of the channel region. To minimize the programming voltage required to cause tunnelling to the floating gate, it is desired to have C2 greater than C1 so that most of the voltage drop between line 47 and the channel region occurs across C1. Because Mori does not use a self aligned floating gate, his C1 is larger than the C1 of the Vora cell described in this patent application, because the Vora cell does not have the two additional parasitic capacitors that raise the capacitance of C1. Therefore, Vora's programming voltage will be lower than Mori's, and this is a significant property of the Vora cell which gives it a significant advantage over the prior art Mori cell along with its greater density.

The "on said substrate" and "over said surface" and "on the surface" Limitations Of Claims 1 And 3-5, Respectively, Defining The Location Of The Bit Line As Above The Surface Of The Substrate Have Not Been Given Proper Weight, And the Mori Reference's Technical Content Has Been

Misint rpr t d

The Examiner has also misinterpreted the claim limitations defining the structure of the bit lines in all the claims. Claim 1 requires that the bit line contact comprise

> "a layer of conductive material formed *on* said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed *in* said substrate."

Earlier in claim 1, the location of the drain region relative to the top surface of the substrate was specified by the following limitation:

> "a vertical MOS transistor formed by alternating N-type and P-type doped layers *in* said substrate..."

The intended and correct meaning for these limitations in light of the specficiation and drawings is a bit line which is *formed completely on top of the substrate which makes contact with the drain region formed in the substrate of the vertical MOS device at every cell.* This is what the drawings of this patent application show for the only embodiments disclosed and this is what the specification describes for the Vora cell. There is no broadening language in the specification that indicates the bit line may also be buried or formed in the substrate.

The Examiner has rejected claims 1 and 3-5 as being anticipated or obvious from the contactless array structure of Mori shown in Figures 1a and 1b.

The Examiner has misconstrued the Mori reference's teachings of a contactless array in stating:

> "A bit line contact 34a comprising a layer of conductive material in contact to drain layer 34 is assumed inherent to Mori's disclosure, as

> Mori shows an opening in insulating layer GO for said contact (Col. 5, lines 35-37, and Figure 1a), and such contact is necessary for the proper functioning of the device. *Thus, Mori discloses all the structural elements of claim 1.* (Emphasis mine)

The Examiner's conclusion that all structural elements of claim 1 are shown in the Mori contactless structure of Figure 1a is incorrect. First, Mori does not have a self aligned floating gate. Second, Mori's contactless array of Figure 1a does not have a bit line which is formed above the top surface of the substrate and which makes contact at every vertical MOS transistor location in the array, as called for by all of claims 1 and 3-5.

The Mori contactless array shown in Figure 1a teaches a buried bit line 34 to which electrical contact is made only at the end of the row. To a skilled artisan, this means that there is no bit line running along the whole row above the surface of the substrate and making contact with the drain of each vertical MOS transistor in the row. The reasons an artisan would draw this conclusion which is different than the Examiner's conclusion from the Mori specification and drawings are as follows.

First, Mori specifically states at Col, 4, lines 48-50 that vertically stacked buried drain bitlines are used in the contactless array. With a buried bit line, there is no need for a bit line formed on the surface. There does need to be contact with the buried bit line, and that is the purpose of the contact window 32a through the GO gate oxide layer at the end of the row. But the presence of this contact window does not mean that there is a bit line on the surface that runs the length of the row and makes contact with every vertical transistor in the row.

The price one pays for a buried bit line is higher resistance. A bit line formed on the surface is exposed and can be metal or can be polysilicon with silicide deposited on

top thereof. Both of these options are lower resistance than a buried doped bit line. Neither metal nor silicide can be used to lower the resistance of a buried bit line. Lower resistance means a lower RC time constant in charging up all the parasitic capacitances coupled to the bit line. This means the voltage on the low resistance bit line on the surface of the substrate can be changed more rapidly to cause an effect in the sense amplifier than is the case for a higher resistance buried bit line. This translates to shorter access time for the surface bit line structure than for the buried bit line structure.

Besides the fact that a buried bit line cannot be covered with silicide nor made of metal, there is the additional fact that the buried bit line of Mori will have periodic restrictions in the cross-sectional area through which current flows at the site of each trench. The reason for this is the buried bit line must act as a drain region at each trench but also must provide a continuous conductive path from each trench to the next. Thus, the bit lines must be slightly wider than the trench at the location of each trench so that the trench does not cut the conductive path. Mori teaches this at Col. 8, lines 53-57 where Mori teaches that the width of the trenches must be selected to be narrower than the width of the source and drain bit lines so that the source and drain bitlines provide a continuous conductive path along the respective row. This means that narrow "runners" of conductive material of the drain bit line will run along the sides of each trench.

These narrow runners act as choke points for the current and raise the overall resistance of the bit line. The formula for the resistance of a conductive layer in an integrated circuit is:

$$R = \rho_s * \frac{L}{W}$$

where R is the resistance of the path;

ρ_s = the sheet resistance of the conductive material in ohms per square; and

L = the length of the conductor and

W = the width of the conductor.

Artisans recognize that the narrow runners increase the resistance. In fact, if the narrow runners each had a resistance of 400 to 800 ohms where the resistance of the bit line segments between the trenchs was 20 ohms, and there were 1000 cells in each row, the bit line resistance across the total row would be in the megohms, and the array would be inoperative as an EEPROM memory.

Thus, Mori's contactless array cell does not teach all the elements, as properly interpreted, claimed in the rejected claims so the anticipation rejection of claims 1 and 3-5 is respectfully requested to be withdrawn.

A Bit Line On The Surface Of A Substrate Need Not Be Wider Than The Trench And Can Lead To A Denser Array

There is another advantage in putting a bit line on the surface of the substrate. That advantage is that the bit line need not be formed to be wider than the trenches as in Mori. This can lead to greater array density because of less spacing between rows since no space between rows is taken up by the runners and suitable safety margins to prevent registration errors from rendering the chip inoperative.

S lf Align d Is Not A Proc ss Limitation

The Examiner took the position that the modifier self aligned for the floating gate limitation is a process limitation. This is not true, and the undersigned respectfully request reconsideration of this position. A self aligned gate in the planar MOS transistor world has definite structural meanin in that the drain and source region edges will be precisely aligned with the edges of the oxide spacers at the edges of the gate.

Likewise, a self aligned floating gate in a vertical transistor now has structural meaning in that the modifier defines a gate with vertical components on the walls of the well only with no horizontal components at the bottom of the well or over the top surface of the substrate.

Further, because the Mori floating gate is formed with a mask, there is a distinct possibility that the edges of the floating gate will extend beyond the edge of the well depending upon the mask configuration and any registration errors with the mask that defined the trench location and size.

The Structure Of The Examiner's Obviousness Rejection Is Improper

The Examiner stated that it would have been obvious to modify the Mori reference to add:

> "a bit line contact to the transistor drain extending into opening 34a disclosed by Mori. The rationale is as follows: one of ordinary skill in the art at the time the invention was made would have been motivated to do so as such bit line contact was necessary for operation of the memory cell."

This does not provide a proper showing of evidence of motivation or suggestion to modify the primary reference. Motivation or suggestion is supported by something in the prior art references or the general level of skill that suggests a particular combination of

elements from two or more references or a particular modification of a primary reference along the lines of the invention claimed would have a reasonable liklihood of success in solving the problem solved by the invention. In re Newell, 13 USPQ2d 1248, 1250 (Fed. Cir. 1989) ["The motivation to make a specific structure is not abstract, but practical, and is always related to the properties or uses one skilled in the art would expect the structure to have, if made."]; In re Gurley, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994) [a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discourage from following the path set out in the reference, or would be led in a direction divergent fromthe path that was taken by the applicant. In general, a reference will teach away if it suggests tha the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant.]

Here, there was no motivation or suggestion provided by the prior art to modify the Mori contactless array of Figure 1a to provide a bit line totally above the surface. This is because the Mori contactless array of Figure 1a already has a buried bit line and does not need another one on the surface. The Examiner is not allowed to make bald conclusions of the existence of suggestion or motivation to make a combination or modification. The Examiner must be able to point to specific evidence in the prior art that supports his or her conclusion of the existence of suggestion or motivation. In re Jones, 21 USPQ2d 1941, 1944 (Fed. Cir. 1992).

Nor is there suggestion proven by the Examiner to modify the Mori reference to make the floating gate self aligned as that term is used in the claims. The Examiner is not allowed to read nonexistent technical description into a reference and cannot read importance of a factor into a reference if the reference itself does not assign importance

to the factor. In re Rijckaert, 28 USPQ2d 1955 (Fed. Cir. 1994). Here, there is no description of a self aligned floating gate in Mori nor is there a recognition of the problem of extra parasitic capacitance caused by the horizontal components. Mori also does not recognize the problems of degradation of array density by using a mask to define the extents of the floating gates and assigns no importance whatsoever to having no horizontal components of the floating gate. If the prior art fails to recognize the problem solved by the invention, an artisan would not be motivated by the reference to solve the unmentioned problem. In re Nomiya, 184 USPQ 607 (CCPA 1975).

There is enclosed herewith a Declaration under 37 CFR 1.132 of Madhu Vora providing evidence to overcome the prima facie obviousness case if the prima facie obviousness case was ever established. Mr. Vora did a sample layout of the Mori cell and Vora cell using industry standard design rules for 1 micron and 0.35 microns. The Mori cell was laid out with the teachings of the Mori contactless cell from the patent. Mr. Vora concludes that the Vora cell on the average is about 3 times smaller than the Mori cell and the array for a 1 square centimeter die is approximately 3-4 times as dense. The principal reasons are the used of a self aligned gate in the Vora cell, and the lack of an isolation barrier and buried layer source implants. The Vora cell does not used buried layer source implants. Instead, the entire substrate has a doped N- layer that serves as the source which is grounded thereby eliminating the need for isolation barriers. The use of the self aligned gate is a large contributor to the small size of the Vora cell.

The Examiner is respectfully requested for the privilege of an in-person or personal interview and is respectfully requested to withdraw all currently pending rejections.

All claims are believed to be in condition for allowance, and favorable action is ernestly solicited.

Respectfully submitted,

Dated: June 9, 1998

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231
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